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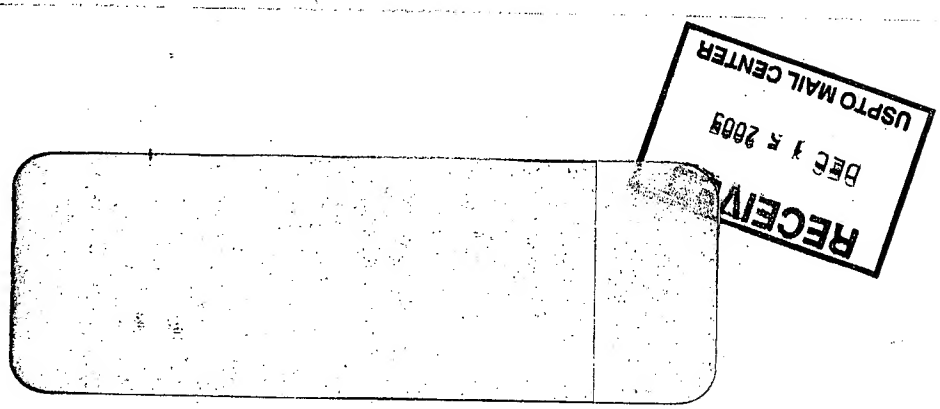

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,795	10/11/2001	Kazuya Ono	A319-1	7244

466 7590 12/14/2005

YOUNG & THOMPSON
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EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,795	ONO, KAZUYA	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *2,7,11 and 16* is/are withdrawn from consideration.

5)☒ Claim(s) *6,8,9,21 and 25* is/are allowed.

6)☒ Claim(s) *1,3-5,10,12-15,17-20,22-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Claim Rejections - 35 USC § 112

1. In view of the recent amendments the rejection of claims 3 and 12, under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, has been withdrawn.

Claim Objections

2. In view of the recent amendments the objection of claim 6 has been withdrawn.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 10, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Götze et al., U.S. Patent 4,450,561, and further in view of Carlton et al., U.S. Patent 4,218,742.

Referring to claim 1:

a. In Figure 2, Götze et al. disclose generating check bits from data. However, Götze et al. don't explicitly disclose having before the byte selection logic a parallel bus interface circuit that receives as an input *m* bit wide data from the parallel bus and multiplexes the *m* bit wide data into sequentially generated *n* bit wide parallel data segments, with $n < m$. The Examiner takes Official Notice that it is well known in the art of communications to use multiplexers and

demultiplexers to convert data streamed on one size bus to data streamed on a different size bus. It would have been obvious to one of ordinary skill at the time of the invention to include a multiplexer and demultiplexer into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because a multiplexer and demultiplexer is simple logic that makes the system more dynamic in that different size buses can be used. Being able to use different size buses enables components operating at different speeds to work together.

b. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence and in column 3, lines 19-20, Götze et al. disclose that the check bits are generated byte-wise (a check bit producer that receives as an input the *n* bit wide parallel data segments and produces as an output a parallel arrangement of the *n* bit wide parallel data segments and a generated error correcting code).

c. In Figure 4, Götze et al. disclose outputting the check bits in parallel, however, Götze et al. don't explicitly disclose a parallel-serial converter, which converts, said parallel arrangement of the *n* bit wide parallel data segments and the error correcting code from said check bit producer into serial data. In column 1, lines 12-18, Carlton et al. disclose that various arrangements are known in the art fro transferring data which is received at a disk file controller in parallel by bit form to a disk file in serial by bit form to be written on one of the tracks. It would have been obvious to one of ordinary skill at the time of the invention to include

the parallel-serial conversion of Carlton et al. into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to include ECC bits when writing and reading data to insure data integrity. Therefore, ECC bits of Götze et al. would be needed in the system of Carlton et al. Further, the system of Carlton et al. provides a means of changing the parallel ECC bits into a serial stream that can be used by most disk drives.

Referring to claim 10:

a. In Figure 2, Götze et al. disclose generating check bits from data. However, Götze et al. don't explicitly disclose having before the byte selection logic a parallel bus interface circuit that receives as an input *m* bit wide data from the parallel bus and multiplexes the *m* bit wide data into sequentially generated *n* bit wide parallel data segments, with $n < m$. The Examiner takes Official Notice that it is well known in the art of communications to use multiplexers and demultiplexers to convert data streamed on one size bus to data streamed on a different size bus. It would have been obvious to one of ordinary skill at the time of the invention to include a multiplexer and demultiplexer into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because a multiplexer and demultiplexer is simple logic that makes the system more dynamic in that different size buses can be used. Being able to use different size buses enables components operating at different speeds to work together.

b. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence and in column 3, lines 19-20, Götze et al. disclose that the check bits are generated byte-wise (applying an error correcting code to each *n* bit wide parallel data segment).

c. In Figure 4, Götze et al. disclose outputting the check bits in parallel, however, Götze et al. don't explicitly disclose converting said parallel data with the error correcting code into serial data. In column 1, lines 12-18, Carlton et al. disclose that various arrangements are known in the art fro transferring data which is received at a disk file controller in parallel by bit form to a disk file in serial by bit form to be written on one of the tracks. It would have been obvious to one of ordinary skill at the time of the invention to include the parallel-serial conversion of Carlton et al. into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to include ECC bits when writing and reading data to insure data integrity. Therefore, ECC bits of Götze et al. would be needed in the system of Carlton et al. Further, the system of Carlton et al. provides a means of changing the parallel ECC bits into a serial stream that can be used by most disk drives.

Referring to claims 19 and 22, in column 3, lines 24-25, Götze et al. disclose that the data word is to comprise eight data bytes having eight data bits each ($n = 8$) and in column 4, lines 15-18, Götze et al. disclose the width of the bus being 4 bytes ($m = 32$).

5. Claims 3, 4, 12, 13, 15, 17, 20, 23, 24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rub, U.S. Patent 6,804,805 B2.

Referring to claim 3:

a. In column 6, lines 15-19, Rub discloses that the parallel-to-serial converter receives the successive ECC code words, converts each ECC code word into a serial representation and concatenates the serial representations to produce a serial stream of ECC code word bits (serial data with an error correcting code transmitted through a serial bus). Further, in column 6, lines 41-44, Rub discloses that the serial-parallel converter groups the bits into ECC code words and converts the ECC code words from a serial format to a parallel format (a serial-parallel converter which converts serial data with an error correcting code transmitted through said serial bus into parallel arrangement of *n* bit wide parallel data segments and the error correcting code).

b. In column 6, lines 46-55, Rub discloses that the ECC code words are sent to an ECC decoder and correction circuit to determine whether any of the ECC symbols contains an error (an error detector which checks the error correcting code within said parallel data).

c. In column 6, lines 59-64, Rub discloses that the data field is then stripped from the recovered ECC code word to recover the original block of data code words, which is then provided to decoder. Bit-level decoder uses the inverse of the coding rules used by encoder to decode the successive data code words into respective data words. However, Rub doesn't explicitly disclose a parallel bus

interface circuit that demultiplexes the *n* bit wide parallel data segments from the error detector into *m* bit wide parallel data on the parallel bus, where $m > n$. The Examiner takes Official Notice that it is well known in the art of communications to use multiplexers and demultiplexers to convert data streamed on one size bus to data streamed on a different size bus. It would have been obvious to one of ordinary skill at the time of the invention to include a multiplexer and demultiplexer into the system of Rub. A person of ordinary skill in the art would have been motivated to make the modification because a multiplexer and demultiplexer is simple logic that makes the system more dynamic in that different size buses can be used. Being able to use different size buses enables components operating at different speeds to work together.

Referring to claim 4, in column 6, lines 55-58, Rub discloses that as long as the number of symbols containing an error is not greater than the maximum number of symbols that can be corrected, the original ECC symbols are recovered (wherein said error detector has a function of correcting said error when said error is detected by said error detector).

Referring to claim 12:

a. In column 6, lines 15-19, Rub discloses that the parallel-to-serial converter receives the successive ECC code words, converts each ECC code word into a serial representation and concatenates the serial representations to produce a serial stream of ECC code word bits (serial data with an included error correcting code). Further, in column 6, lines 41-44, Rub discloses that the serial-parallel

converter groups the bits into ECC code words and converts the ECC code words from a serial format to a parallel format (converting serial data with an included error correcting code into parallel arrangement of *n* bit wide parallel data segments and the error correcting code).

b. In column 6, lines 46-55, Rub discloses that the ECC code words are sent to an ECC decoder and correction circuit to determine whether any of the ECC symbols contains an error (checking the error correcting code applied to each said parallel data segment checking for an error based on said error correcting code).

c. In column 6, lines 59-64, Rub discloses that the data field is then stripped from the recovered ECC code word to recover the original block of data code words, which is then provided to decoder. Bit-level decoder uses the inverse of the coding rules used by encoder to decode the successive data code words into respective data words. However, Rub doesn't explicitly disclose demultiplexing the *n* bit wide parallel data segments into *m* bit wide parallel data on the parallel bus, wherein $m > n$. The Examiner takes Official Notice that it is well known in the art of communications to use multiplexers and demultiplexers to convert data streamed on one size bus to data streamed on a different size bus. It would have been obvious to one of ordinary skill at the time of the invention to include a multiplexer and demultiplexer into the system of Rub. A person of ordinary skill in the art would have been motivated to make the modification because a multiplexer and demultiplexer is simple logic that makes the system more

dynamic in that different size buses can be used. Being able to use different size buses enables components operating at different speeds to work together.

Referring to claim 13, in column 6, lines 55-58, Rub discloses that as long as the number of symbols containing an error is not greater than the maximum number of symbols that can be corrected, the original ECC symbols are recovered (the step of correcting said error detected in said error checking step).

Referring to claim 15:

a. In column 6, lines 15-20, Rub discloses that the parallel-to-serial converter receives the successive ECC code words and converts each ECC code word into a serial representation and concatenates the serial representations to produce a serial stream of ECC code word bits (applying an error correcting code to each parallel data segment; and converting each said parallel data segment with the error code into serial data. However, Rub doesn't explicitly disclose multiplexing *m* bit wide parallel data from the parallel bus into *n* bit wide segments, where $m > n$.

b. In column 6, lines 42-49, Rub discloses that serial-to-parallel converter groups the bits into ECC code words and converts the ECC code words from a serial format to a parallel format. Serial-to-parallel converter then outputs the successively recovered ECC code words in parallel format to ECC decoder and correction circuit (converting serial data with included error codes transmitted through said serial bus into parallel arrangement of the *n* bit wide parallel data segments and the error correcting code.

c. In column 6, lines 46-55, Rub discloses that the ECC code words are sent to an ECC decoder and correction circuit to determine whether any of the ECC symbols contains an error (checking the error correcting code applied to each parallel data segment).

d. In column 6, lines 59-64, Rub discloses that the data field is then stripped from the recovered ECC code word to recover the original block of data code words, which is then provided to decoder. Bit-level decoder uses the inverse of the coding rules used by encoder to decode the successive data code words into respective data words. However, Rub doesn't explicitly disclose a parallel bus interface circuit that demultiplexes the *n* bit wide parallel data segments from the error detector into *m* bit wide parallel data on the parallel bus, where $m > n$.

e. With reference to the limitations above that aren't taught by Rub. The Examiner takes Official Notice that it is well known in the art of communications to use multiplexers and demultiplexers to convert data streamed on one size bus to data streamed on a different size bus. It would have been obvious to one of ordinary skill at the time of the invention to include a multiplexer and demultiplexer into the system of Rub. A person of ordinary skill in the art would have been motivated to make the modification because a multiplexer and demultiplexer is simple logic that makes the system more dynamic in that different size buses can be used. Being able to use different size buses enables components operating at different speeds to work together.

Referring to claim 17, in column 6, lines 55-58, Rub discloses the correction of errors by using the ECC symbols (said error detector has a function of correcting said error when said error is detected by said error detector).

Referring to claims 20, 23, and 24, in column 5, lines 4-5, Rub discloses that each data word can include any number of bits (m = 32 and n = 8).

Referring to claim 26, in Figure 2, Rub discloses that the n bit wide segments transferred while communicating from the parallel bus to the serial bus follow a different path than that used to transfer the n bit wide data segments while communicating from the serial bus to the parallel bus.

6. Claims 5, 14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rub, U.S. Patent 6,804,805 B2, and further in view of Götze et al., U.S. Patent 4,450,561.

Referring to claims 5, 14, and 18, in column 6, lines 55-58, Rub discloses that as long as the number of symbols containing an error is not greater than the maximum number of symbols that can be corrected, the original ECC symbols are recovered. However, Rub doesn't explicitly disclose that said error detector corrects said error when said error is a 1-bit error, and abandons an access when said error is a 2-bit error. In column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector corrects said error when said error is a 1-bit error). Further, in column 6, lines 39-42, Götze et al. disclose that a double error can be detected but not corrected (said error detector abandons an access when said error is a 2-bit error). It would have been obvious to

skill at the time of the invention to include the correction of 1-bit errors and the abandonment of 2-bit errors of Götze et al. into the system of Rub. A person of ordinary skill in the art would have been motivated to make the modification because it is well-known that most ECC devices are structured in such a manner that single errors can be corrected (see Götze et al.: column 3, lines 4-6) and it is common for double errors to be difficult to correct because of the inability to find the bits that are incorrect (see Götze et al.: column 6, lines 31-42 and Rub: column 6, lines 55-59).

Allowable Subject Matter

7. Claims 6, 8, 9, 21, and 25 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter.

Referring to claim 6, the prior art does not teach or reasonably suggest, in combination with all the limitations, that the parallel bus interface is also connected to receive as an input the parallel data segments from the error detector, the parallel bus interface demultiplexing the *n* bit wide parallel data segments from the error detector into *m* bit wide parallel data on the parallel bus.

Response to Arguments

9. Applicant's arguments, filed October 21, 2005, with respect to the rejection(s) of claim(s) 3, 4, 12, 13, 20, and 23 under 35 U.S.C. 102(e) as being anticipated by Rub have been fully considered and are persuasive. Therefore, the rejection has been

withdrawn. However, upon further consideration, a new ground(s) of rejection has been made.

10. Applicant's arguments, filed October 21, 2005, with respect to the rejection(s) of claim(s) 1, 10, 19, and 22 under 35 U.S.C. 103(a) as being unpatentable over Götze et al., and further in view of Carlton et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection has been made.

11. Applicant's arguments, filed October 21, 2005, with respect to the rejection(s) of claim(s) 5, 14, 15, 17, 18, 24, and 26 under 35 U.S.C. 103(a) as being unpatentable over Rub, and further in view of Götze et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection has been made.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited art is related to the use of multiplexers and demultiplexers in converting different width buses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Maskulinski

Michael C Maskulinski
Examiner
Art Unit 2113

Notice of References Cited	Application/Control No. 09/973,795	Applicant(s)/Patent Under Reexamination ONO, KAZUYA	
	Examiner Michael C. Maskulinski	Art Unit 2113	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,848,042 B1	01-2005	Campbell et al.	712/35
*	B	US-6,941,418 B1	09-2005	Goolsby, Jeremy B.	711/109
	C	US-			
	D	US-			
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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